Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.129”**

**PAD FUNCTIONS:**

1. **V IN**
2. **V OUT**
3. **V OUT**
4. **SENSE**
5. **ADJUST**

****

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: B = .007 X .009” min.**

**E = .008 X .008”**

**Backside Potential: COLLECTOR**

**APPROVED BY: DK DIE SIZE .030” X .030” DATE: 2/8/22**

**MFG: FAIRCHILD THICKNESS .008” P/N: 2N3019**

**DG 10.1.2**

#### Rev B, 7/1